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Commissioner for Patents  
Serial No. 10/804,182

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**Amendments to the Claims:**

This listing of claims replaces all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1.-11. (Cancelled)

12. (Currently Amended) A method for accessing a dynamic random access memory (DRAM), the DRAM having a plurality of memory storage elements located arranged in rows and columns, the method comprising steps of:

- a) initiating a first memory access by providing a first address signal indicative of the location of at least one memory storage element to be accessed;
- b) decoding the first address signal to select a row and at least one column corresponding to the location of the at least one memory storage element;
- c) enabling a word line corresponding to the selected row;
- d) activating a sense amplifier to latch data to or from the at least one selected column;
- e) disabling the word line corresponding to the selected row;
- f) precharging the at least one selected column;
- g) initiating a second memory access by providing a second address signal indicative of the location of at least one memory storage element to be accessed; and
- h) decoding the second address signal to select a row and at least one column corresponding to the location of the at least one memory storage element, the second memory access commencing before the step of precharging the selected column has completed.

13. (Previously Amended) A method according to claim 12, wherein the step of decoding the second address signal occurs at substantially the same time as the precharging step.

14. (Previously Amended) A method according to claim 12, wherein the memory storage elements are arranged in a plurality of sub-arrays and the method further comprises decoding the first and second address signals to select at least one sub-array.

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15. (Previously Amended) A method according to claim 12, wherein decoding the first address signal comprises decoding a row address and a column address at substantially the same time.

16. (Previously Amended) A method according to claim 12, wherein decoding the second address signal comprises decoding a row address and a column address at substantially the same time.

17. (Previously Amended) A method according to claim 12, wherein the memory access is one of a read access, a write access, or a refresh access.

18. (Previously Amended) A method according to claim 12, including the step of deriving a plurality of self timed clock pulses from a system clock signal for controlling the timing of steps (b) to (f).

19. (Previously Amended) A method according to claim 12, including the step of performing memory accesses on consecutive cycles of a system clock signal.

20. (Currently Amended) A dynamic random access memory (DRAM) comprising:

- a) a plurality of memory storage elements ~~located~~ arranged in rows and columns, each memory storage element being coupled to a bit line pair and a word line;
- b) a row decoder for decoding ~~a row addresses~~ from an address signals received in respective clock periods and for asserting ~~a word line signals~~ on a word lines corresponding to the decoded row addresses;
- c) a column decoder for decoding ~~a column addresses~~ from the address signals and for selecting at least one corresponding bit line pair;
- d) precharge circuitry for precharging the at least one pair of bit lines; and
- e) timing circuitry for controlling the activation of the precharge circuitry such that the precharging of memory storage elements selected by a first address signal occurs at substantially the same time as a next ~~the~~ address signal is being decoded by the row and

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column decoders regardless of which memory storage elements are selected by the first and next address signals.

21. (Previously Amended) A DRAM according to claim 20, wherein the memory storage elements are arranged in a plurality of sub-arrays, the DRAM further comprising a sub-array decoder for decoding the address signal to provide a sub-array select signal.
22. (Previously Amended) A DRAM according to claim 21, wherein each sub-array comprises a data line, the data line capable of being coupled to the selected bit line.
23. (Previously Amended) A DRAM according to claim 20, wherein the DRAM is an embedded DRAM.
24. (Previously Amended) A DRAM according to claim 20, further comprising an address register for latching the address signal in response to a system clock signal.
25. (Previously Amended) A DRAM according to claim 20, wherein the decoded row address is combined with a word line timing pulse to assert the word line signal on the word line.
26. (Previously Amended) A DRAM according to claim 20, wherein the timing circuitry comprises a delay element that is used to provide a time delayed version of a system clock signal for synchronizing the activation of the precharge circuitry.
27. (Previously Amended) A DRAM according to claim 20, wherein the address signal comprises N bits defining the column address and M bits defining the row address.
28. (Previously Amended) A DRAM according to claim 20, wherein the row decoder and the column decoder decode the address signal at substantially the same time.

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